EE 330
Lecture 16

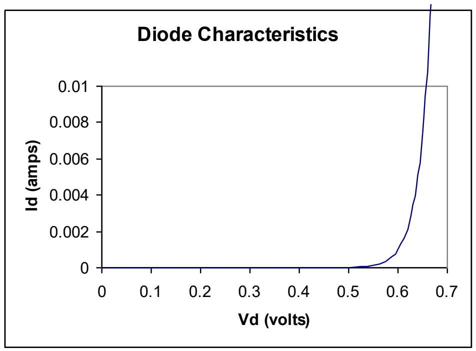
Devices in Semiconductor Processes

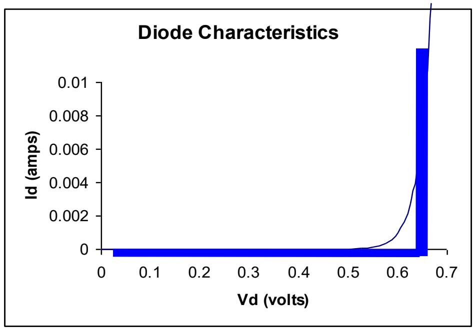
- MOSFETs

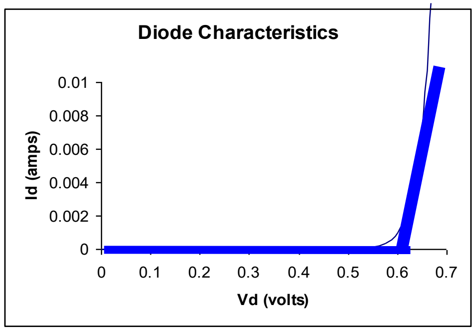
Fall 2025 Exam Schedule

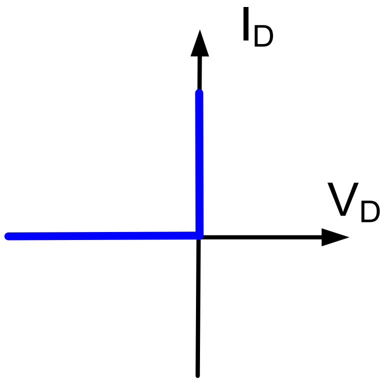
Exam 1	Friday	Sept 26
Exam 2	Friday	October 24
Exam 3	Friday	Nov 21
Final Exam	Monday	Dec 15 12:00 - 2:00 PM

Diode Models









Which model should be used?

The simplest model that will give acceptable results in the analysis of a circuit

Review from Last Lecture

Analysis of Nonlinear Circuits

(Circuits with one or more nonlinear devices)

What analysis tools or methods can be used?

KCL ?

KVL?

~~Superposition?~~

~~Voltage Divider ?~~

~~Current Divider?~~

~~Thevenin and Norton Equivalent Circuits?~~

Nodal Analysis ?

Mesh Analysis ?

Two-Port Subcircuits ?

~~Passing Current ?~~

~~Blocking Current ?~~

- How are piecewise models accommodated?
- Will address the issue of how to rigorously analyze nonlinear circuits with piecewise models later

Review from Last Lecture

Use of Piecewise Models for Nonlinear Devices when Analyzing Electronic Circuits

Process:

1. Guess state of the device
2. Analyze circuit
3. Verify State
4. Repeat steps 1 to 3 if verification fails
5. Verify model (if necessary)

Observations:

- Analysis generally simplified dramatically (particularly if piecewise model is linear)
- Approach applicable to wide variety of nonlinear devices
- Closed-form solutions give insight into performance of circuit
- Usually much faster than solving the nonlinear circuit directly
- Wrong guesses in the state of the device do not compromise solution (verification will fail)
- Helps to guess right the first time
- Detailed model is often not necessary with most nonlinear devices
- Particularly useful if piecewise model is PWL (but not necessary)
- For practical circuits, the simplified approach usually applies

Key Concept For Analyzing Circuits with Nonlinear Devices

Review from Last Lecture

Use of Piecewise Models for Nonlinear Devices when Analyzing Electronic Circuits

Single Nonlinear Device

Process:

1. Guess state of the device
2. Analyze circuit
3. Verify State
4. Repeat steps 1 to 3 if verification fails
5. Verify model (if necessary)

Multiple Nonlinear Devices

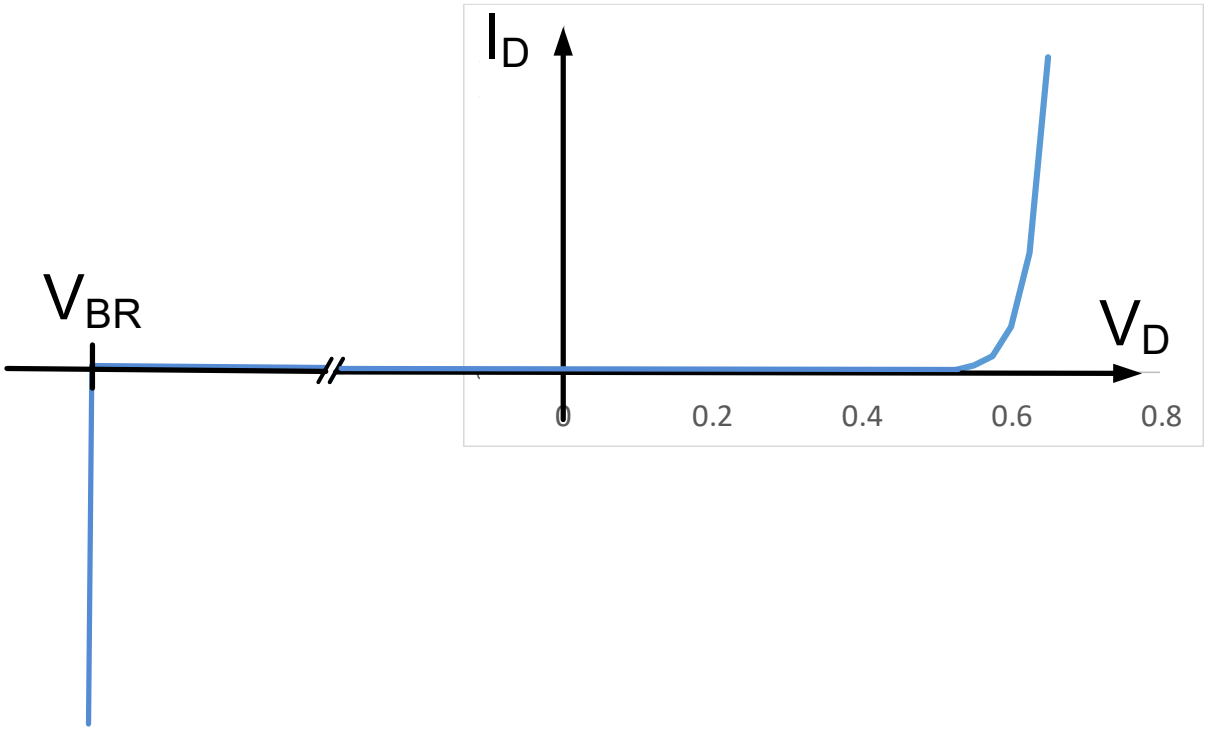
Process:

1. Guess state of each device (may be multiple combinations)
2. Analyze circuit
3. Verify State
4. Repeat steps 1 to 3 if verification fails
5. Verify models (if necessary)

Analytical solutions of circuits with multiple nonlinear devices are often impossible to obtain if detailed non-piecewise nonlinear models are used

Review from Last Lecture

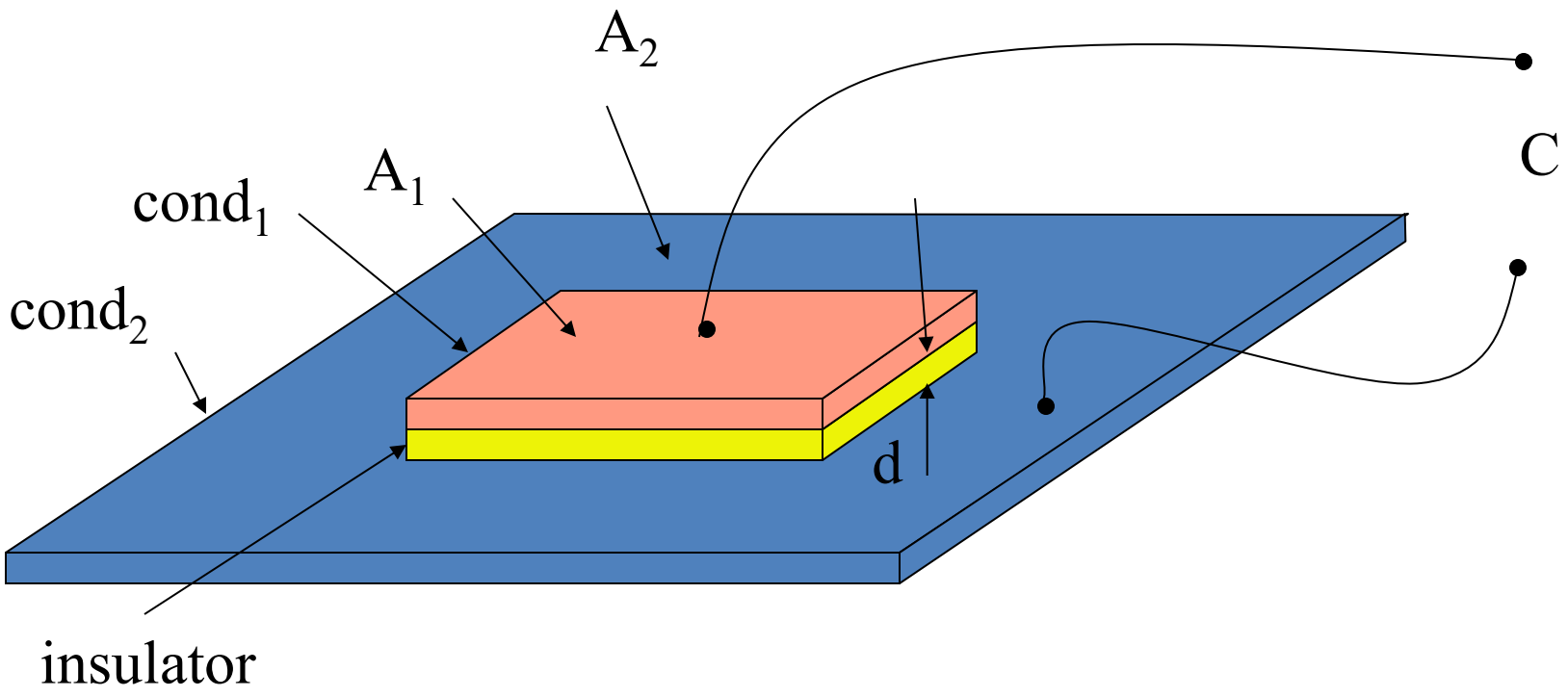
Diode Breakdown



- Diodes will “break down” if a large reverse bias is applied
- Unless current is limited, reverse breakdown is destructive
- Breakdown is very sharp
- For many signal diodes, V_{BR} is in the -100V to -1000V range
- Relatively easy to design circuits so that with correct diodes, breakdown will not occur
- Zener diodes have a relatively small breakdown and current is intentionally limited to use this breakdown to build voltage references

Review from Last Lecture

Parallel Plate Capacitors

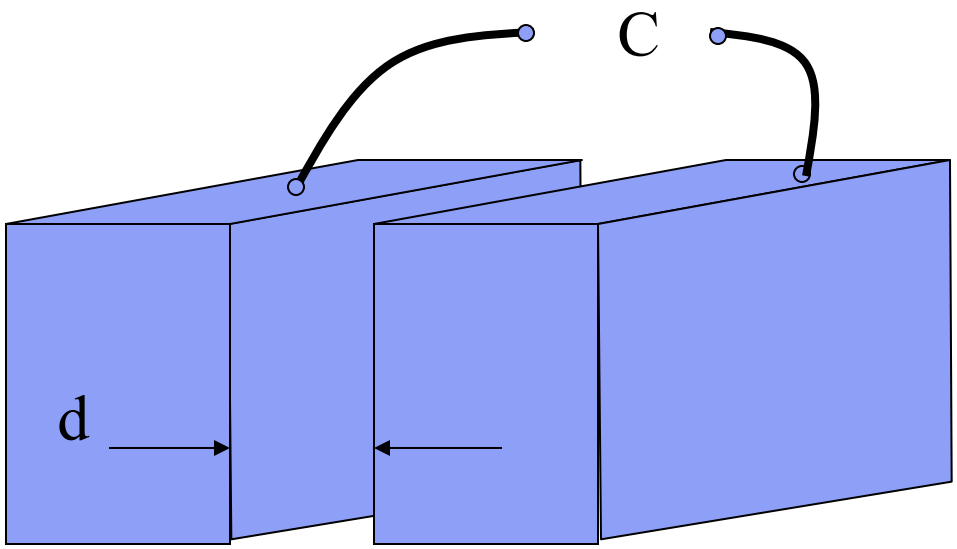


A = area of intersection of A_1 & A_2

One (top) plate intentionally sized smaller to determine C

$$C = \frac{\in A}{d}$$

Fringe Capacitors



$$C = \frac{\varepsilon A}{d}$$

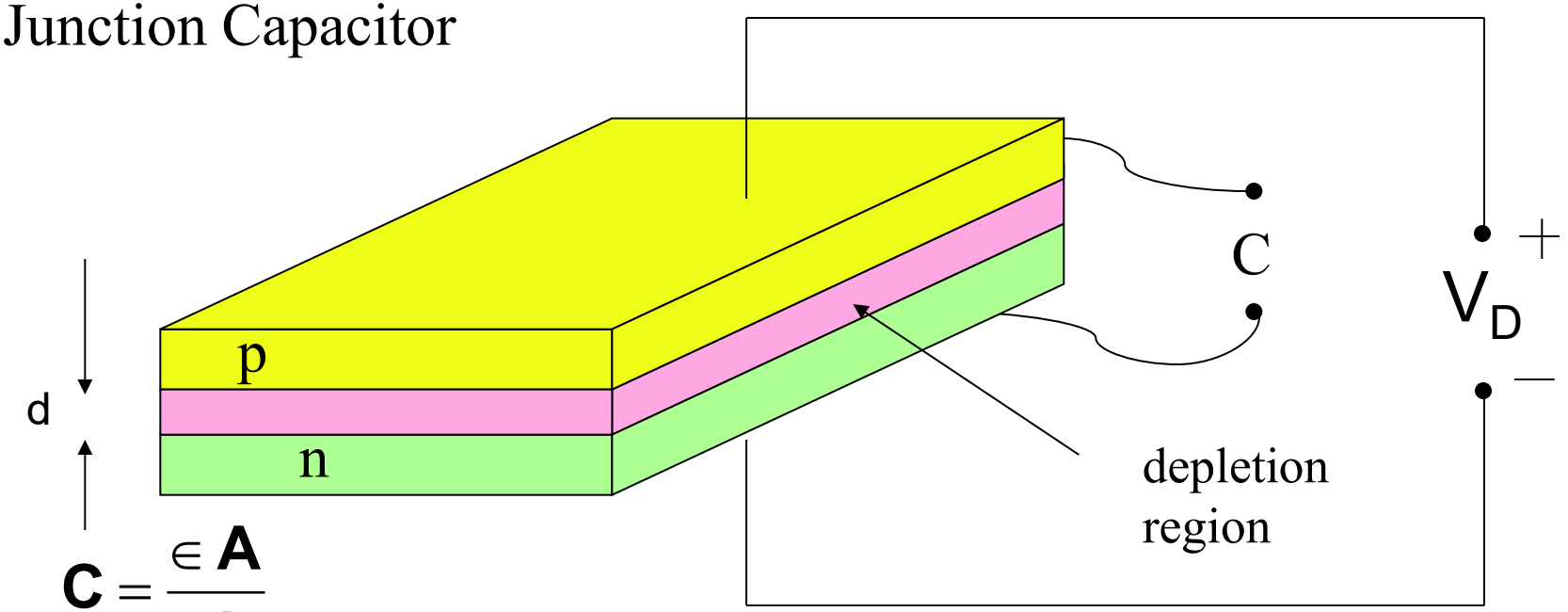
A is the area where the two plates are parallel

Only a single layer is needed to make fringe capacitors

Review from Last Lecture

Capacitance

Junction Capacitor



$$C = \frac{\in A}{d}$$

$\in$ is dielectric constant

$$C = \frac{C_{jo}A}{\left(1 - \frac{V_D}{\varphi_B}\right)^n} \qquad for \ V_{FB} < \frac{\varphi_B}{2}$$

Note: d is voltage dependent
-capacitance is voltage dependent
-usually parasitic caps
-varicaps or varactor diodes exploit voltage dep. of C

C_{j0} is the zero—bias junction capacitance density

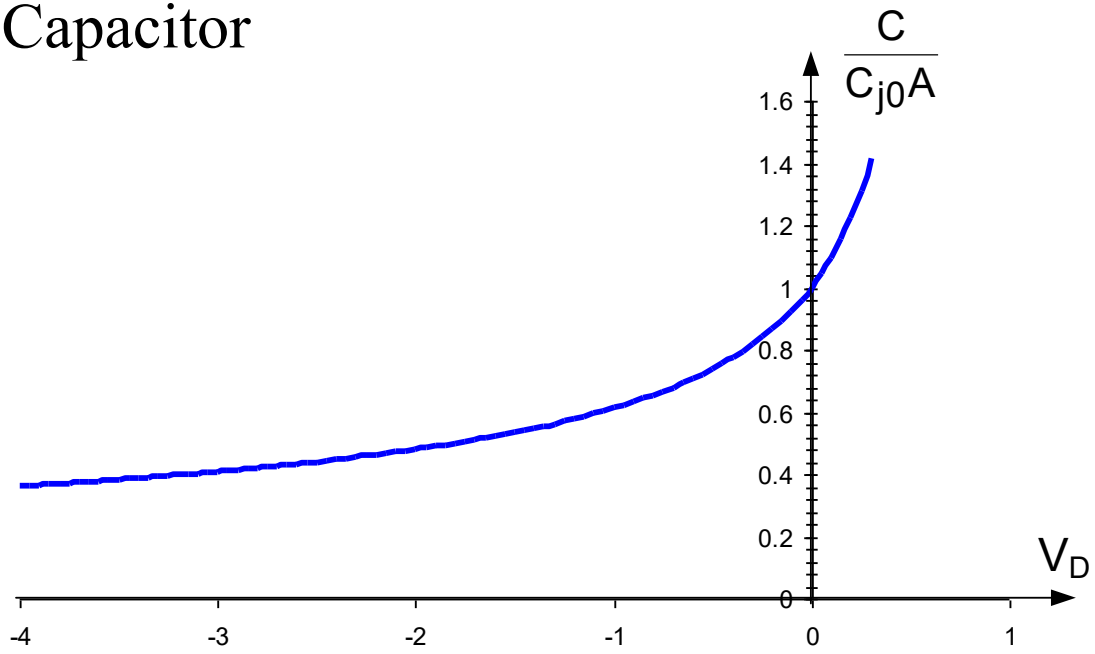
Model parameters $\{C_{jo}, n, \varphi_B\}$ Design parameters $\{A\}$

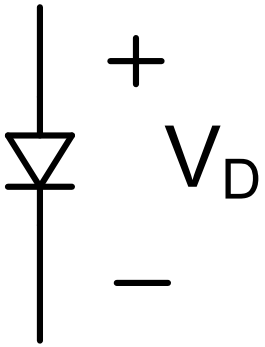
$\varphi_B \cong 0.6V$ $n \simeq 0.5$ C_{jo} highly process dependent around $500aF/\mu m^2$

Review from Last Lecture

Capacitance

Junction Capacitor





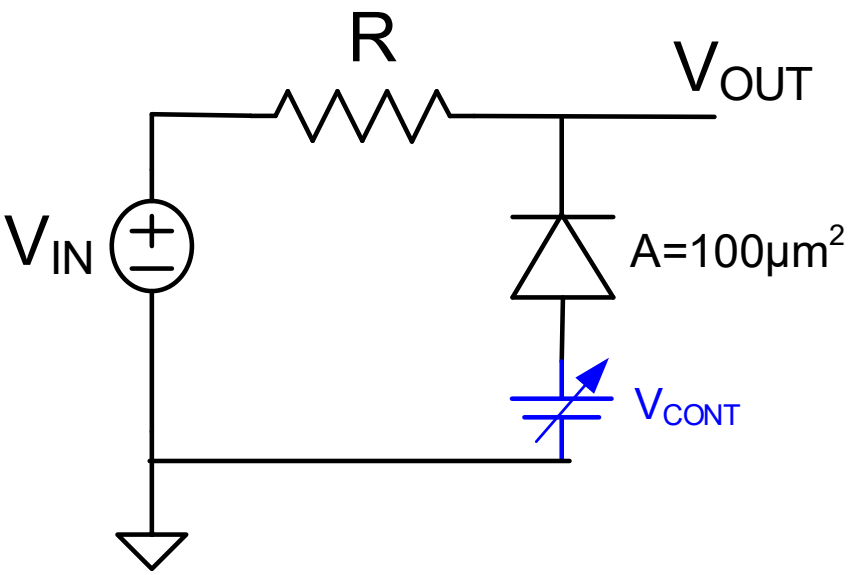
$$C = \frac{C_{jo}A}{\left(1 - \frac{V_D}{\varphi_B}\right)^n} \qquad for \; V_{FB} < \frac{\varphi_B}{2}$$

Voltage dependence is substantial

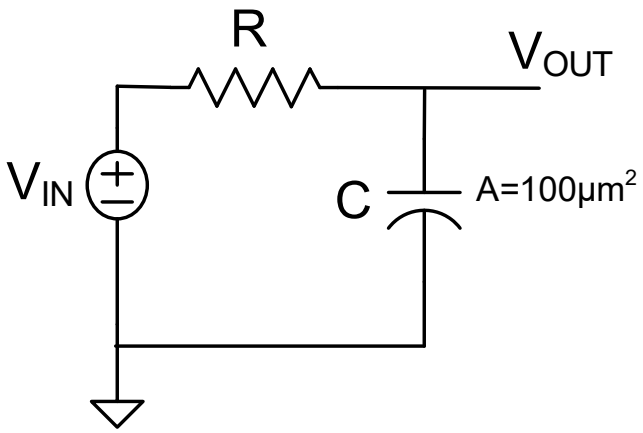
$\varphi_B \cong 0.6V$ $\quad n \simeq 0.5$

Example:

Determine the 3dB frequency of the lowpass filter shown if V_{CONT}=0V and if V_{CONT}=-2V. Assume R=10M, the diode junction area is 100μm^2, and the diode is a p+:n-well diode in the process attached.

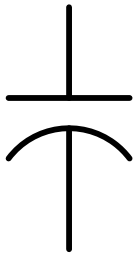


AC equivalent circuit



$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1+RCs}$$

$$BW = \frac{1}{RC}$$



$$C = \frac{C_{jo}A}{\left(1-\frac{V_D}{\varphi_B}\right)^n} \quad for \quad V_{FB} < \frac{\varphi_B}{2}$$

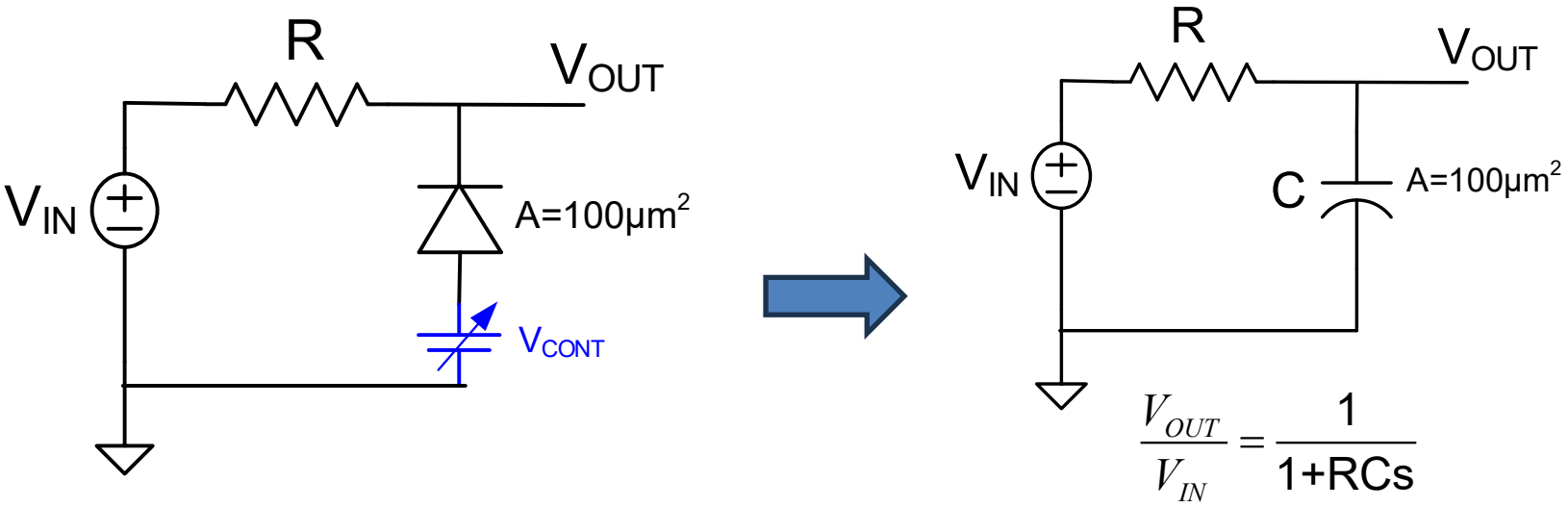
With V_D=0 C_1=37aF μm^{-2} x 100 μm^2 =3.7fF

With V_D=-2V $C_2 = \frac{C_{jo}A}{\left(1-\frac{V_D}{\varphi_B}\right)^n} = \frac{3.7fF}{\left(1+\frac{2V}{0.6V}\right)^{0.5}}$ =1.78fF

CAPACITANCE PARAMETERS	N+	P+	POLY	POLY2	M1	M2	M3	N_W	UNITS
Area (substrate)	425	731	84		27	12	7	37	aF/um^2
Area (N+active)			2434		35	16	11		aF/um^2
Area (P+active)			2335						aF/um^2
Area (poly)				938	56	15	9		aF/um^2
Area (poly2)					49				aF/um^2
Area (metal1)						31	13		aF/um^2
Area (metal2)							35		aF/um^2
Fringe (substrate)	344	238			49	33	23		aF/um
Fringe (poly)					59	38	28		aF/um
Fringe (metal1)						51	34		aF/um
Fringe (metal2)							52		aF/um
Overlap (N+active)			232						aF/um
Overlap (P+active)			312						aF/um

Example:

Determine the 3dB frequency of the lowpass filter shown if V_{CONT}=0V and if V_{CONT}=-2V. Assume R=10M, the diode junction area is 100μm^2, and the diode is a p+:n-well diode in the process attached.



C_1=3.7fF C_2=1.78fF

$$BW = \frac{1}{RC}$$

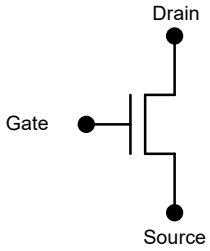
$$BW_1 = \frac{1}{RC_1} = \frac{1}{10M \cdot 3.7fF} = 27M \text{ rad/sec} = 4.3MHz$$

$$BW_2 = \frac{1}{RC_2} = \frac{1}{10M \cdot 1.78fF} = 56M \text{ rad/sec} = 8.9MHz$$

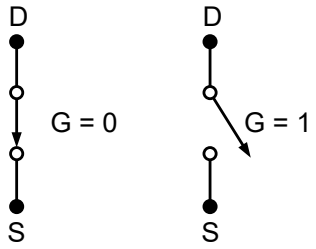
Basic Devices and Device Models

- Resistor
- Diode
- Capacitor
- MOSFET
- BJT

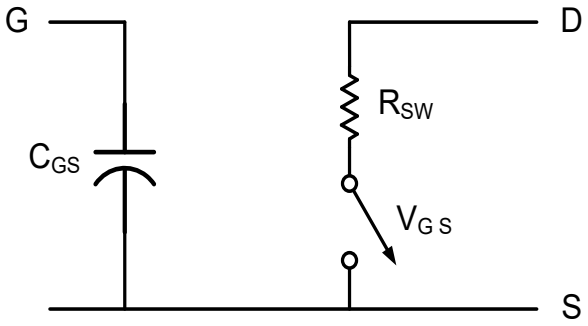
Summary of Existing Models (for n-channel)



1. Switch-Level model



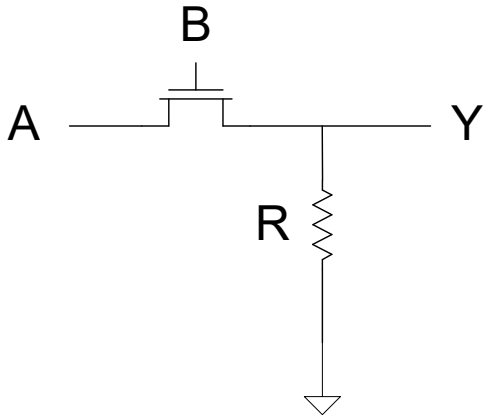
2. Improved switch-level model



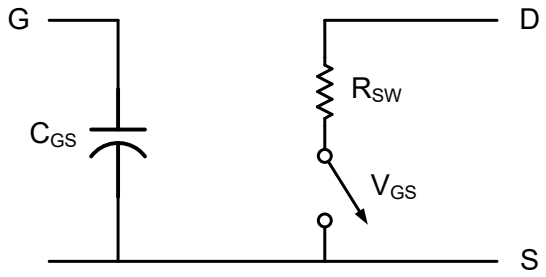
Switch closed for $|V_{GS}|$ *= large*

Switch open for $|V_{GS}|$ *= small*

Limitations of Existing MOSFET Models



What is Y when A=B=VDD

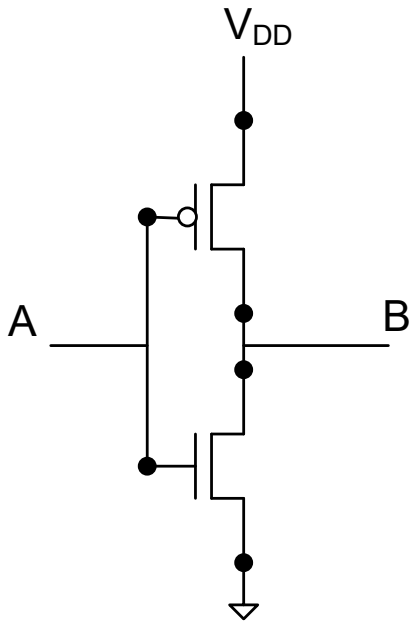


For minimum-sized devices in a 0.5u process with V_{DD}=5V

$$C_{GS} \cong 1.5fF$$

$$R_{sw} \cong \begin{cases} 2K\Omega \;\; n-channel \\ 6K\Omega \;\; p-channel \end{cases}$$

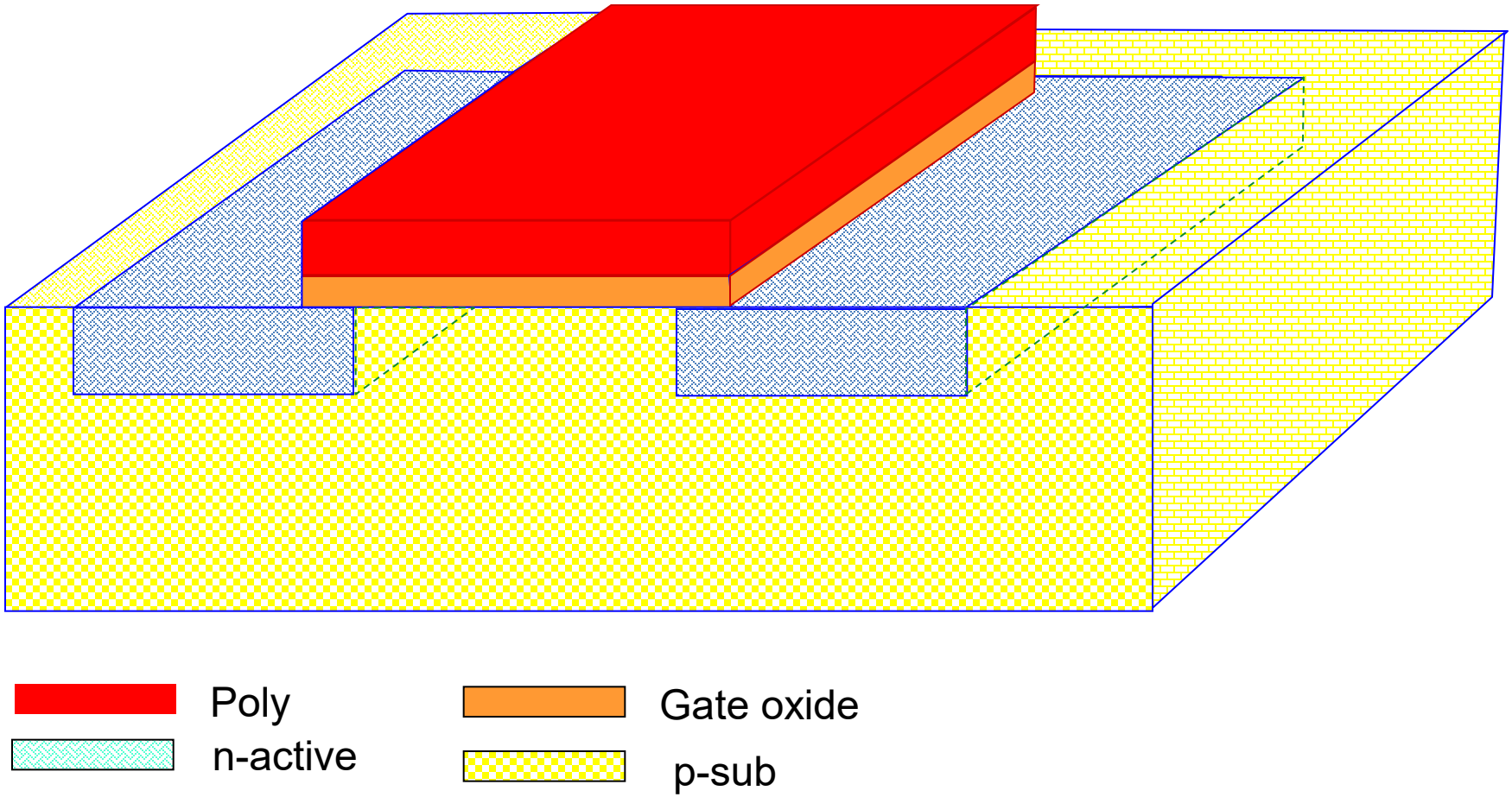
What is R_{SW} if MOSFET is not minimum sized?



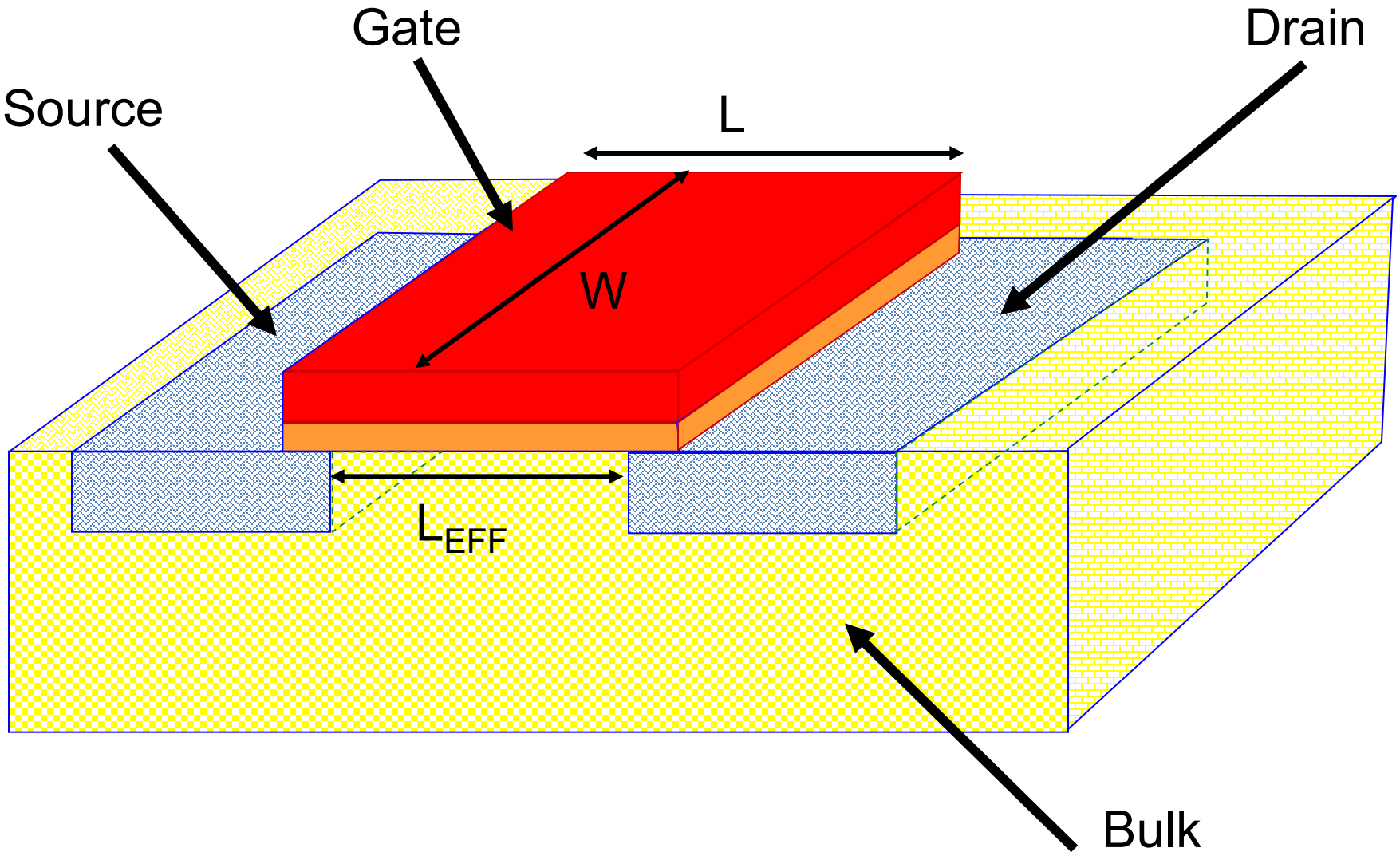
What is power dissipation if A is stuck at an intermediate voltage?

Better Model of MOSFET is Needed!

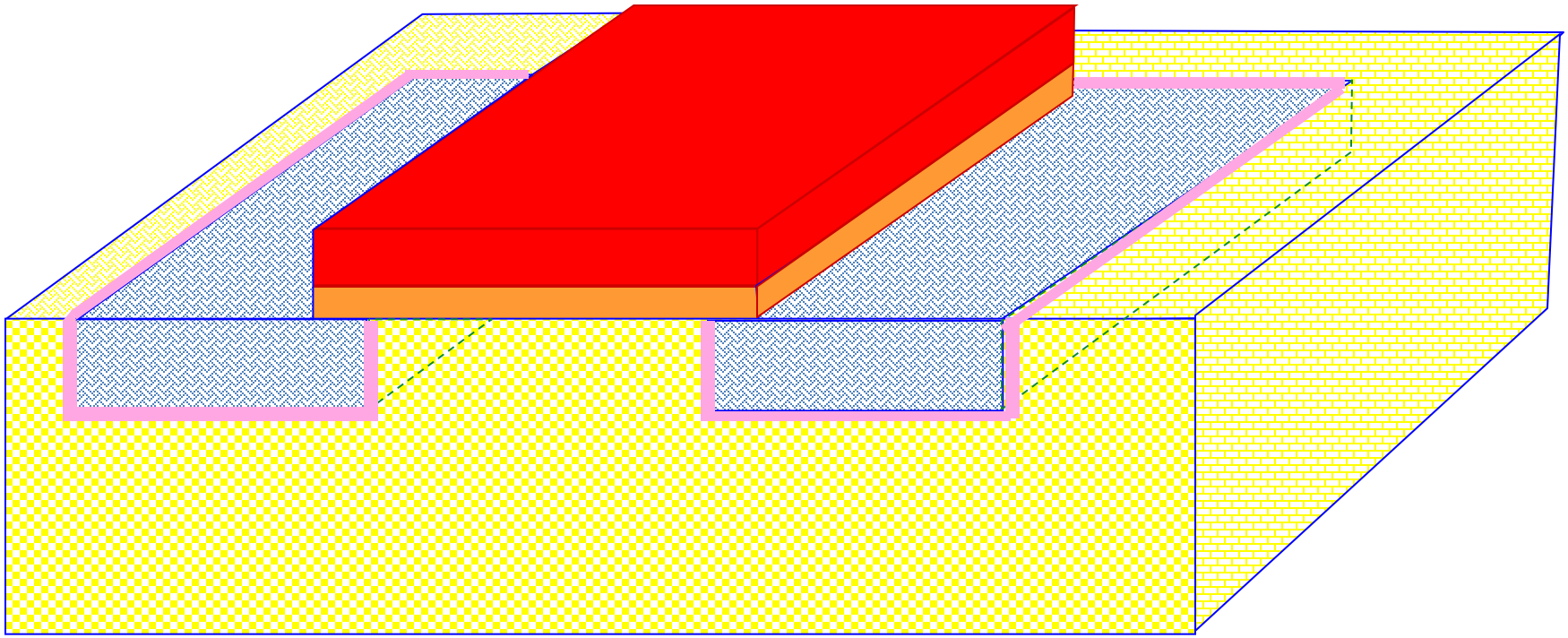
n-Channel MOSFET



n-Channel MOSFET



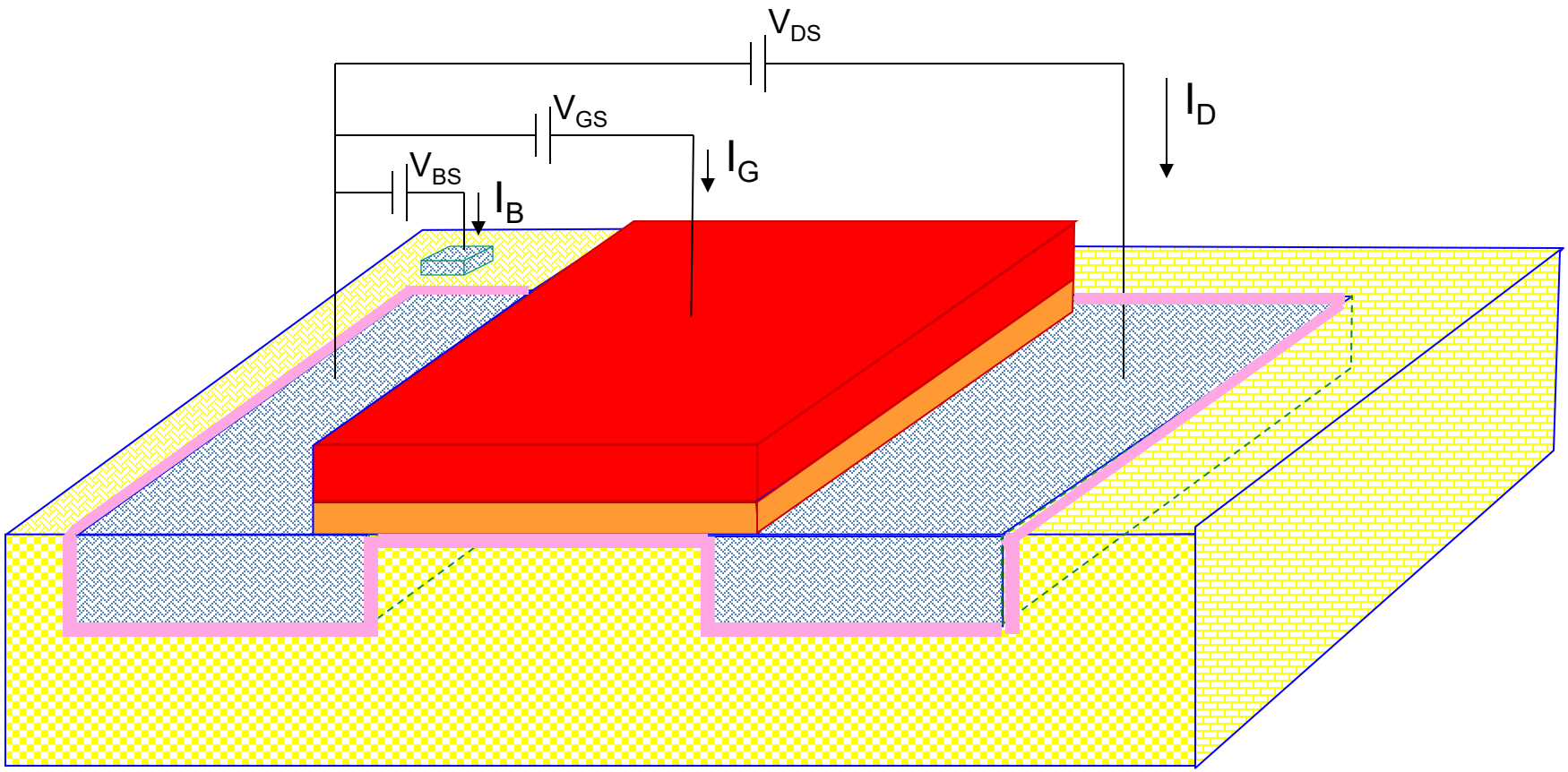
n-Channel MOSFET



Poly
Gate oxide
n-active
p-sub
depletion region (electrically induced)

- In what follows assume all pn junctions reverse biased (almost always used this way)
- Extremely small reverse bias pn junction current can be neglected in most applications

n-Channel MOSFET Operation and Model



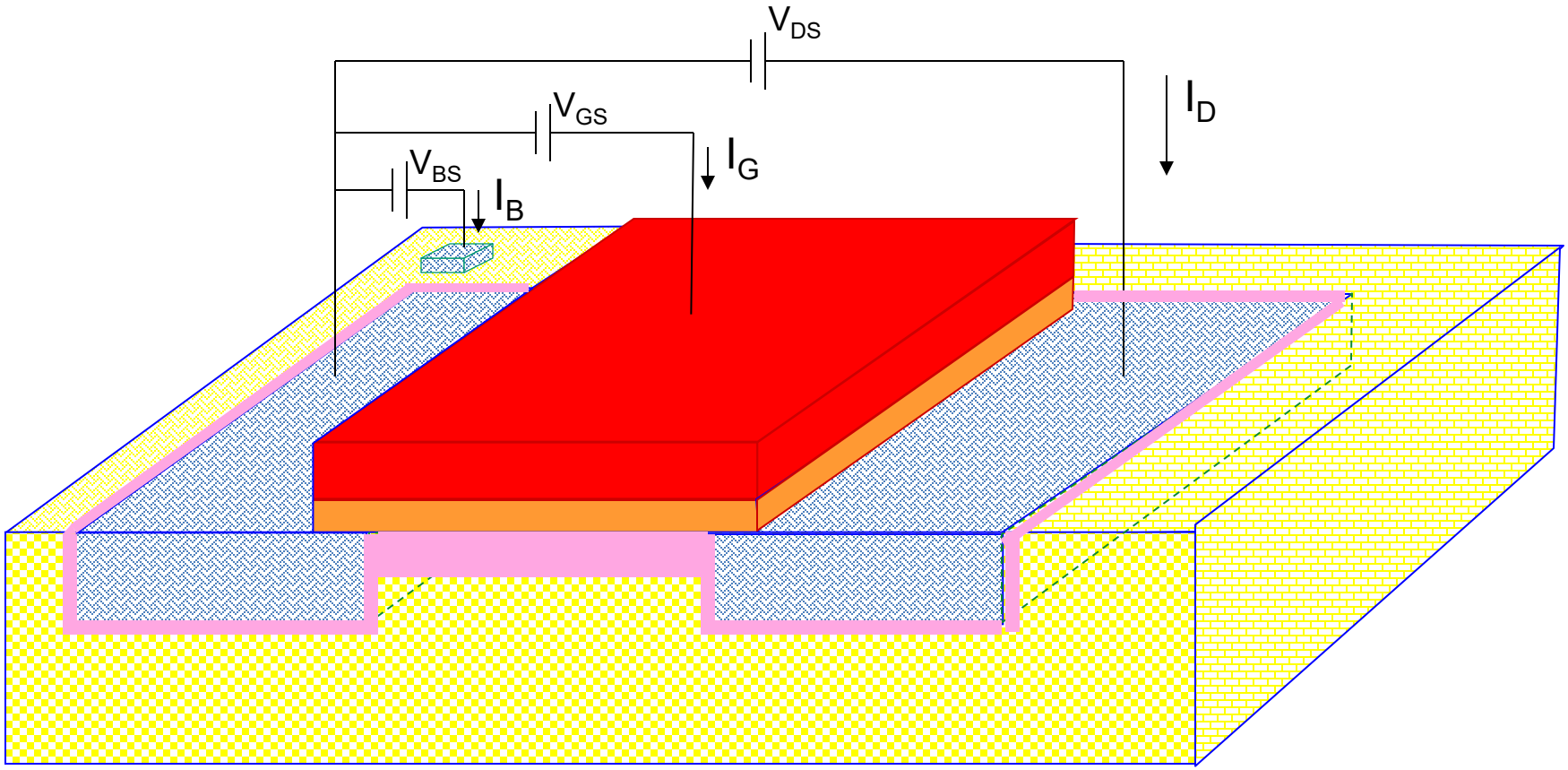
Apply small V_{GS}
(V_{DS} and V_{BS} assumed to be small)

Depletion region electrically induced in channel

Termed “cutoff” region of operation

$I_D=0$
$I_G=0$
$I_B=0$

n-Channel MOSFET Operation and Model

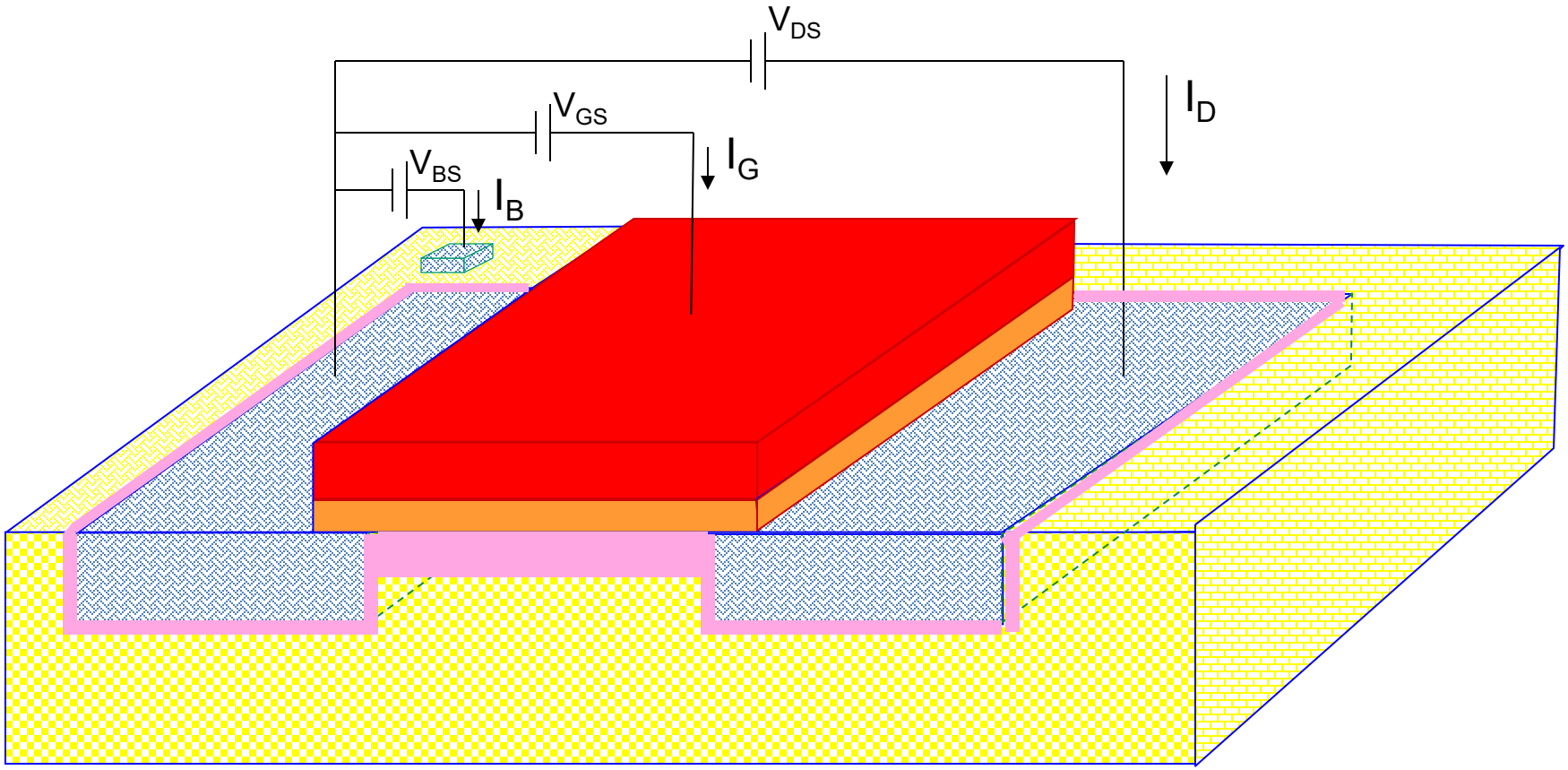


Increase V_{GS}
(V_{DS} and V_{BS} assumed to be small)

Depletion region in channel becomes larger

$I_D=0$
$I_G=0$
$I_B=0$

n-Channel MOSFET Operation and Model

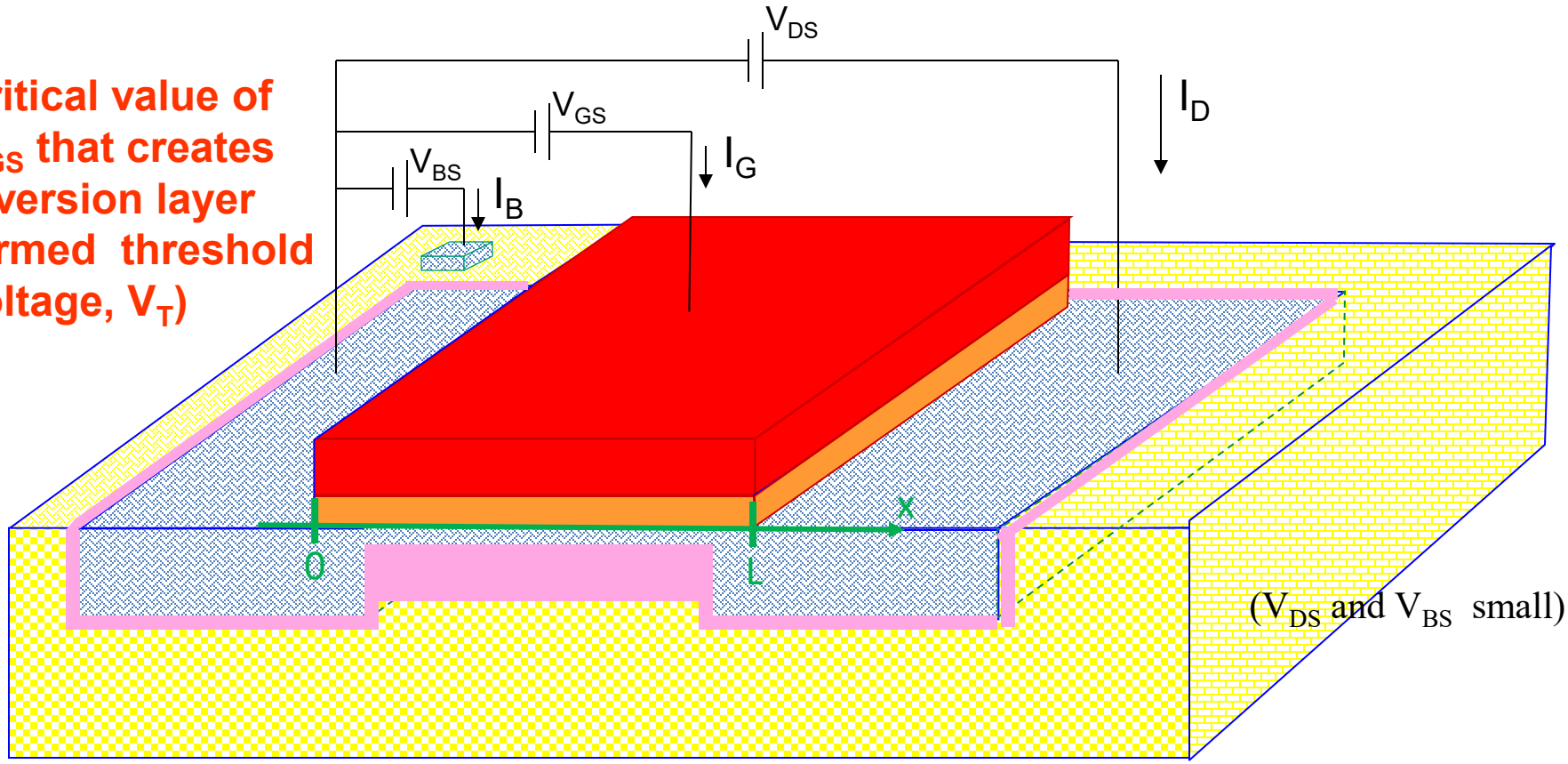


$I_D=0$
$I_G=0$
$I_B=0$

Model in Cutoff Region

n-Channel MOSFET Operation and Model

Critical value of V_{GS} that creates inversion layer termed threshold voltage, V_T)



Increase V_{GS} more

Inversion layer forms in channel

Inversion layer will support current flow from D to S

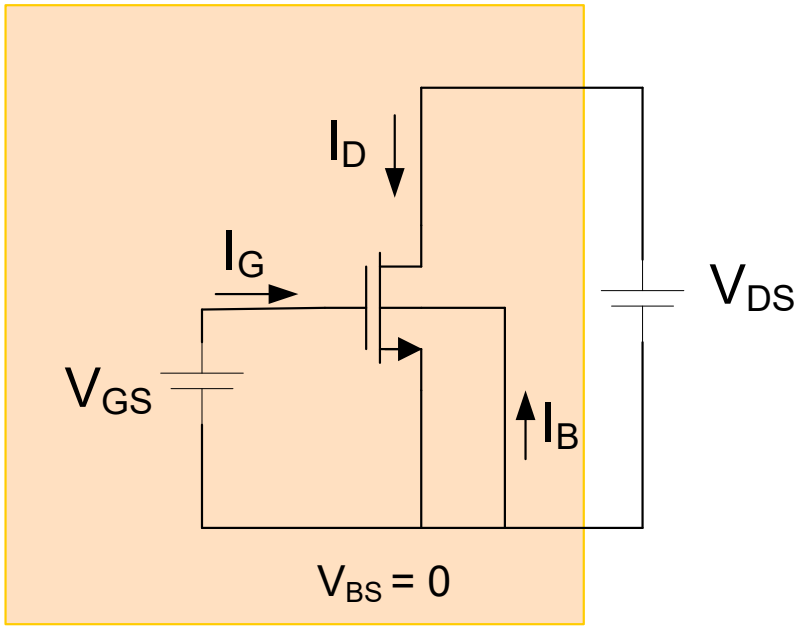
Channel behaves as thin-film resistor

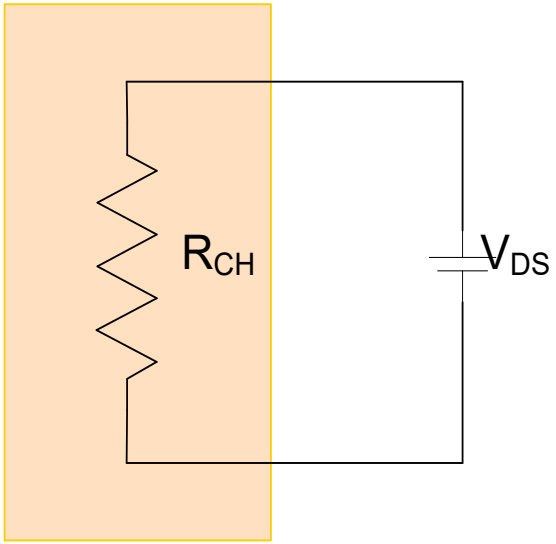
$I_D R_{CH} = V_{DS}$

$I_G = 0$

$I_B = 0$

Triode Region of Operation





For V_{DS} small

$$R_{CH} = \frac{L}{W}\frac{1}{(V_{GS} - V_{TH})\mu C_{OX}}$$

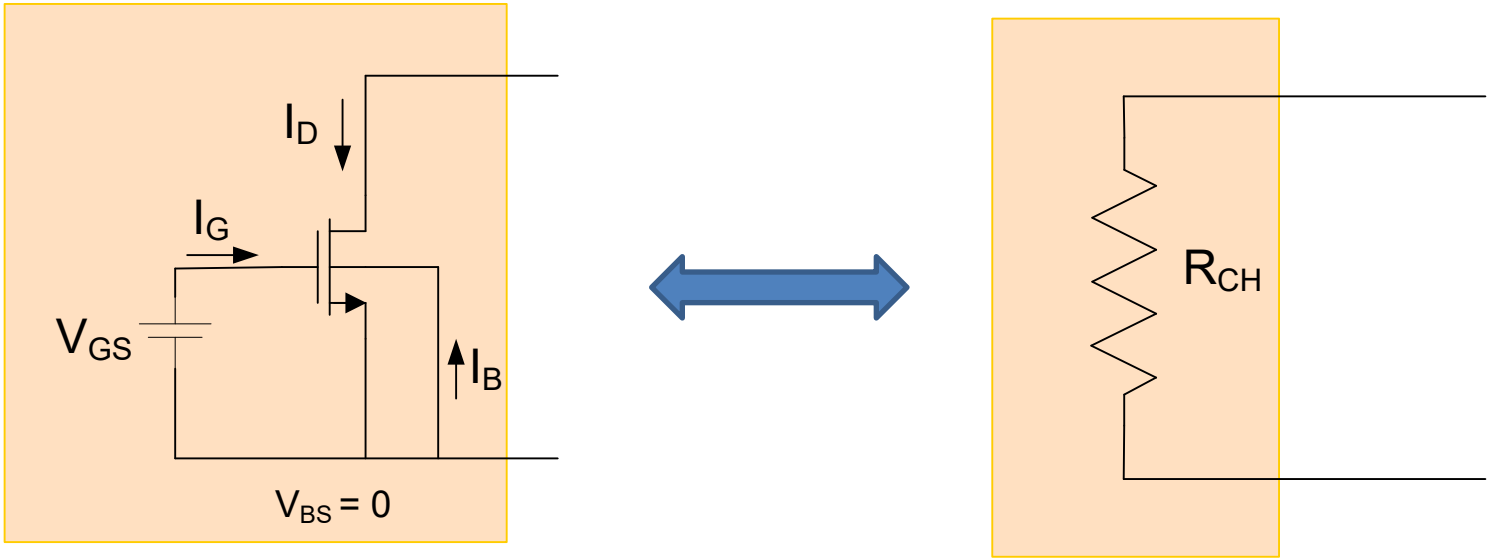
Behaves as a resistor between drain and source

$$I_D = \mu C_{OX}\frac{W}{L}(V_{GS} - V_{TH})V_{DS}$$

$$I_G = I_B = 0$$

Model in Deep Triode Region

Triode Region of Operation

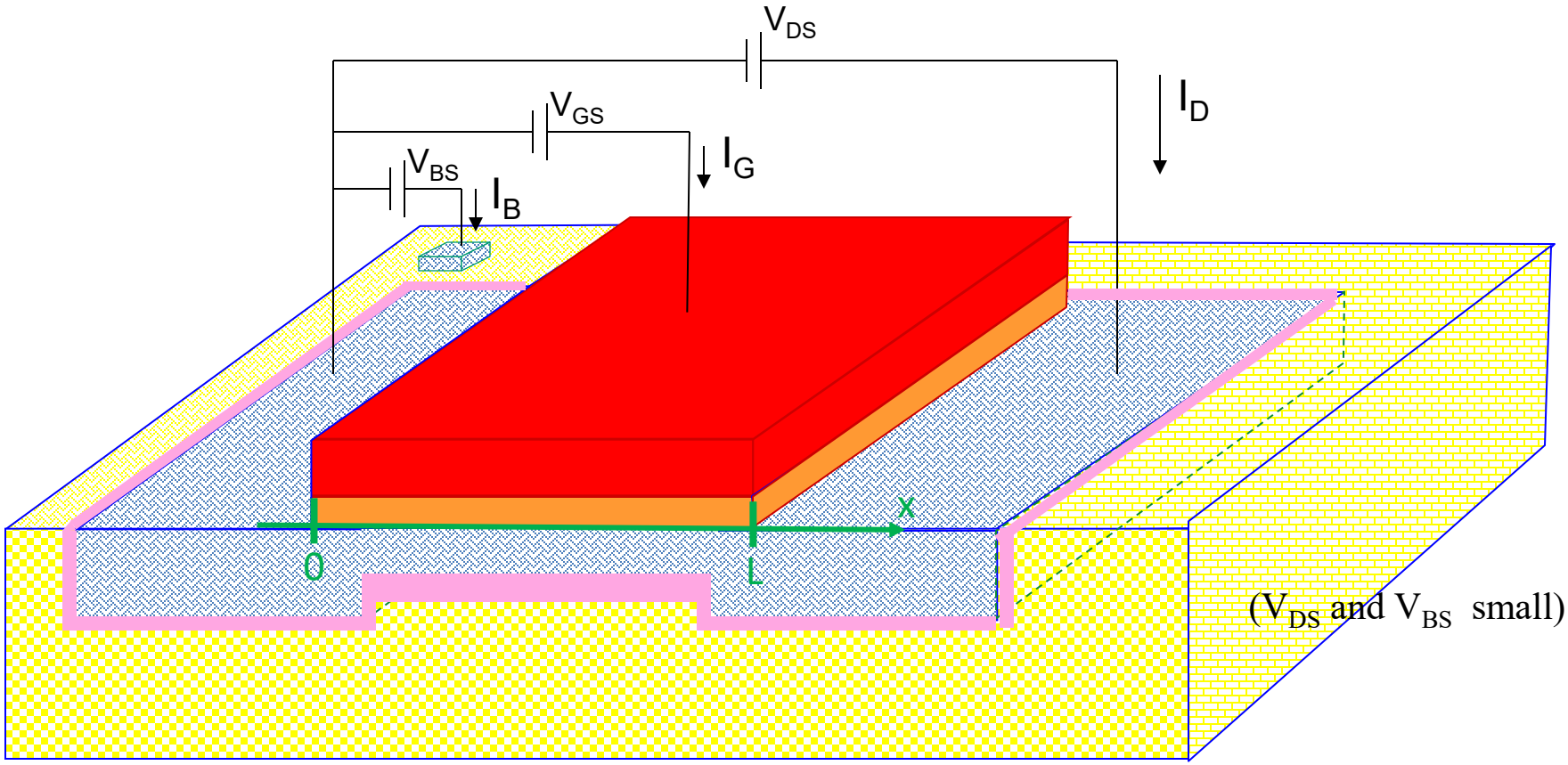


For V_{DS} small

$$R_{CH} = \frac{L}{W} \frac{1}{(V_{GS} - V_{TH})\mu C_{OX}}$$

Resistor is controlled by the voltage V_{GS}
Termed a “Voltage Controlled Resistor” (VCR)

n-Channel MOSFET Operation and Model



$V_{GC}(x)$ approx. constant for small V_{DS}

Increase V_{GS} more (with V_{DS} and V_{BS} still small)

Inversion layer in channel thickens

R_{CH} will decrease

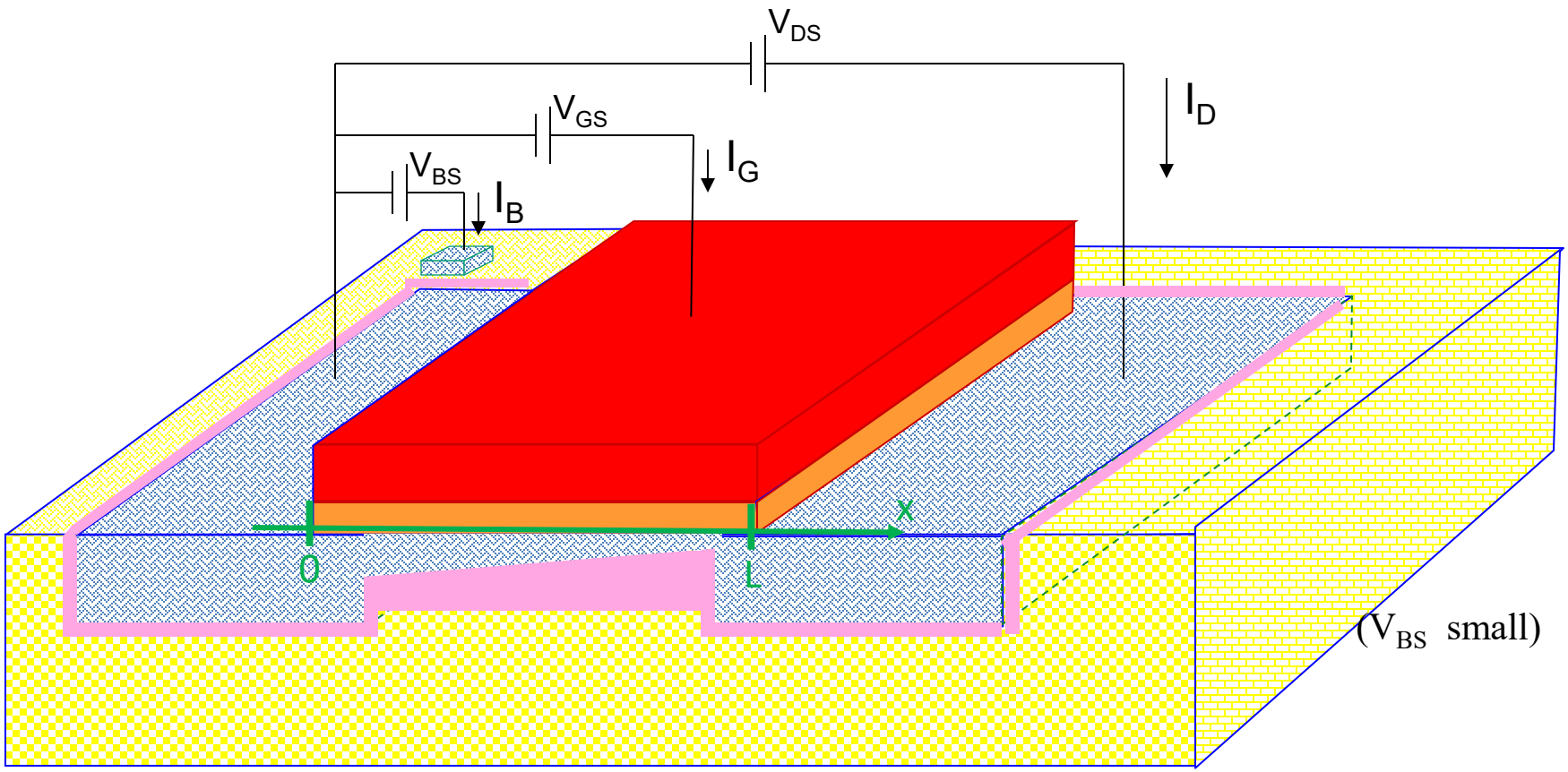
Termed "ohmic" or "triode" region of operation

$I_D R_{CH} = V_{DS}$

$I_G = 0$

$I_B = 0$

n-Channel MOSFET Operation and Model



Increase V_{DS}

$V_{GC}(x)$ changes with x for larger V_{DS}

Inversion layer thins near drain

I_D no longer linearly dependent upon V_{DS}

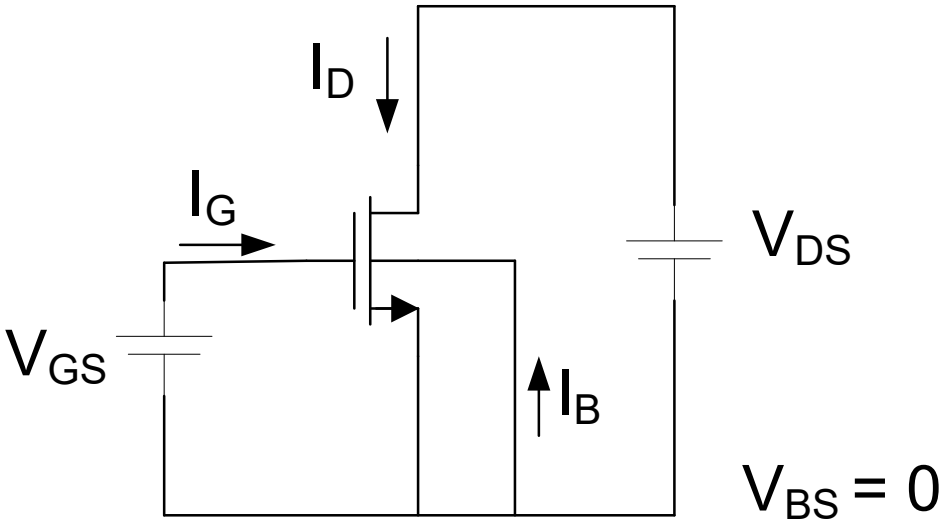
Still termed "ohmic" or "triode" region of operation

I_D=?

I_G=0

I_B=0

Triode Region of Operation



For V_{DS} larger

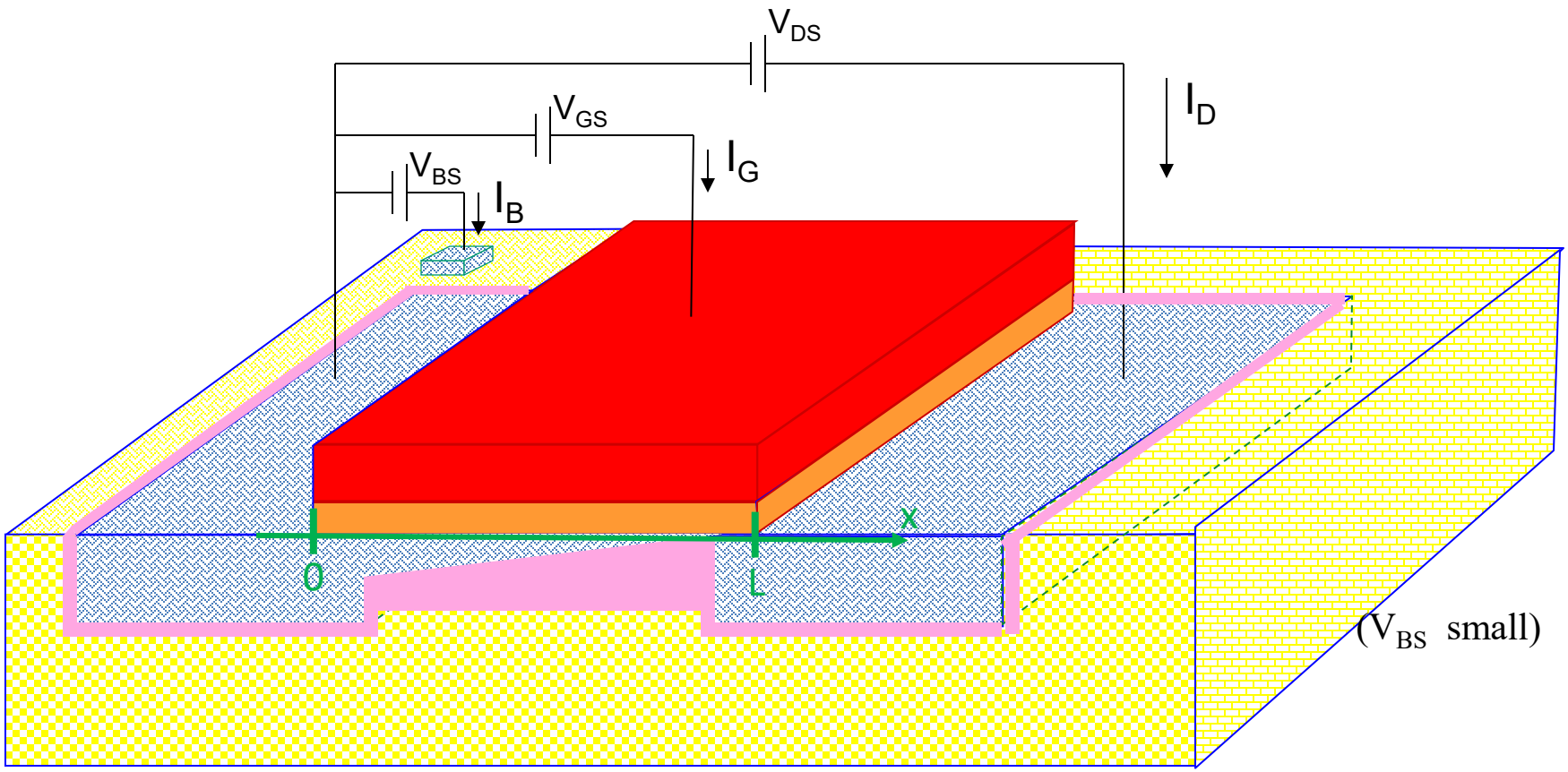
$$R_{CH} = \frac{L}{W} \frac{1}{(V_{GS} - V_{TH})\mu C_{OX}}$$

$$I_D = \mu C_{OX} \frac{W}{L}\left(V_{GS} - V_{TH} - \frac{V_{DS}}{2}\right)V_{DS}$$

$$I_G = I_B = 0$$

Model in Triode Region

n-Channel MOSFET Operation and Model



Increase V_{DS} even more

$V_{GC}(L) = V_{TH}$ when channel saturates

Inversion layer disappears near drain

Termed "saturation"region of operation

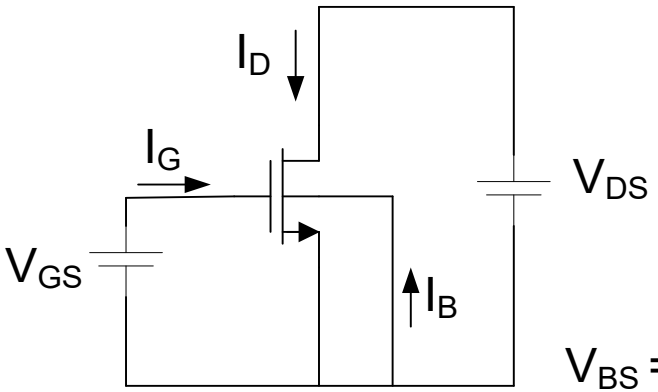
Saturation first occurs when $V_{DS}=V_{GS}-V_{TH}$

$I_D=?$

$I_G=0$

$I_B=0$

Saturation Region of Operation



For V_{DS} at onset of saturation

$$I_D = \mu C_{OX} \frac{W}{L}\left(V_{GS} - V_{TH} - \frac{V_{DS}}{2} \right) V_{DS}$$

or equivalently

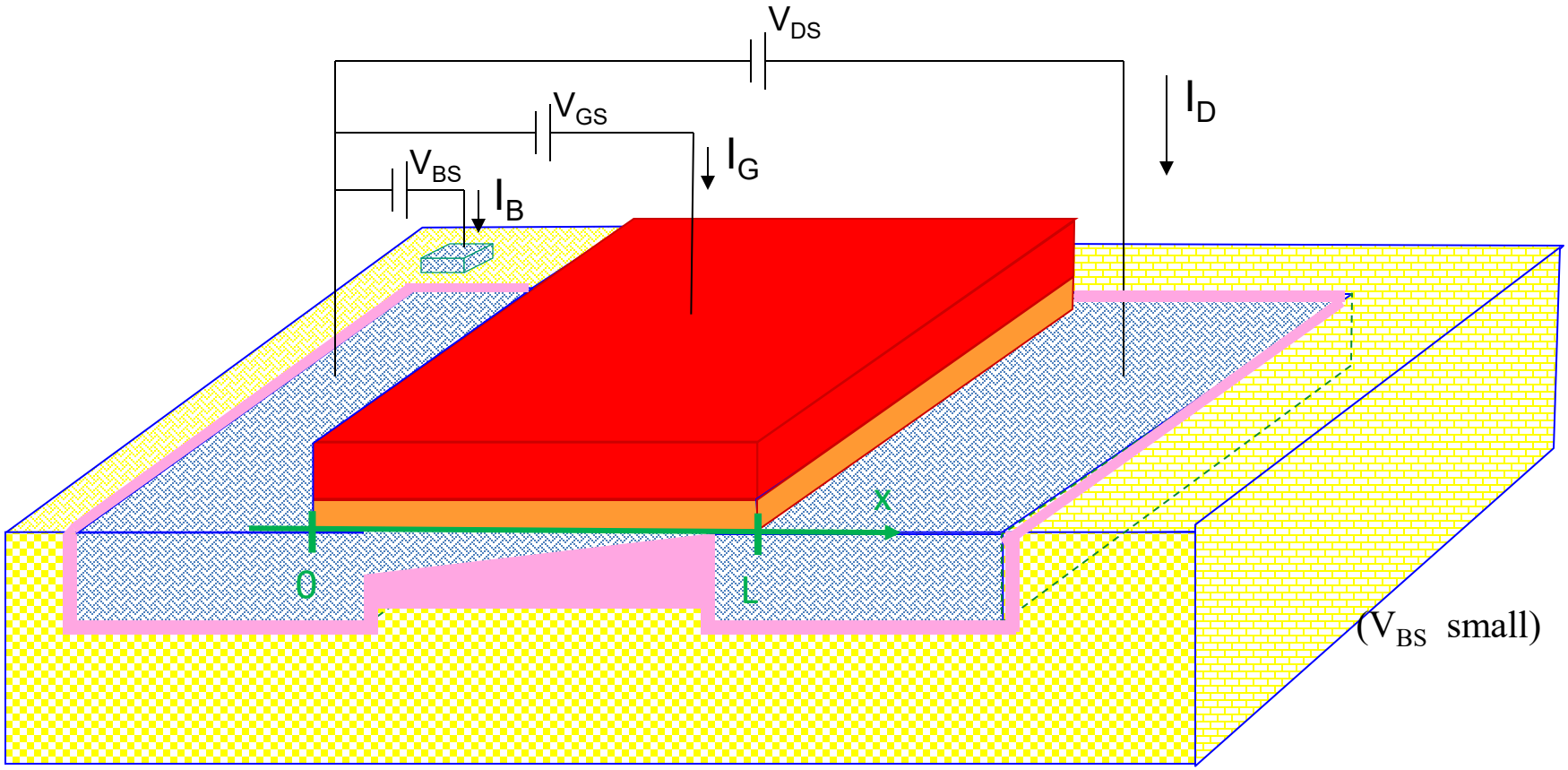
$$I_D = \mu C_{OX} \frac{W}{L}\left(V_{GS} - V_{TH} - \frac{V_{GS} - V_{TH}}{2} \right)\left(V_{GS} - V_{TH} \right)$$

or equivalently

$$I_D = \frac{\mu C_{OX} W}{2L}\left(V_{GS} - V_{TH} \right)^2$$

$$I_G = I_B = 0$$

n-Channel MOSFET Operation and Model



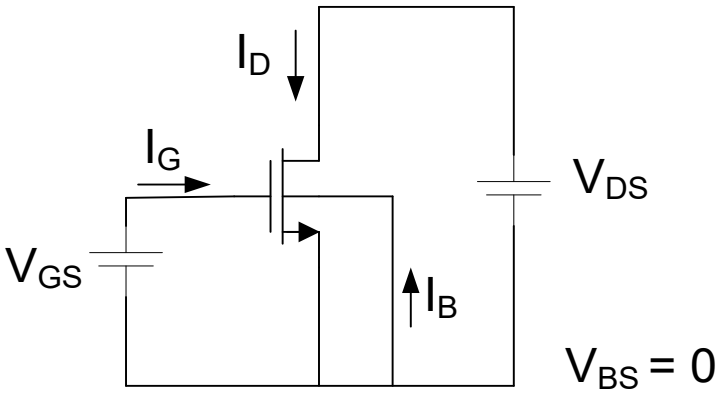
Increase V_{DS} even more (beyond V_{GS}-V_{TH})

Nothing much changes !!

Termed “saturation”region of operation

I_D=?
I_G=0
I_B=0

Saturation Region of Operation



For V_{DS} in Saturation

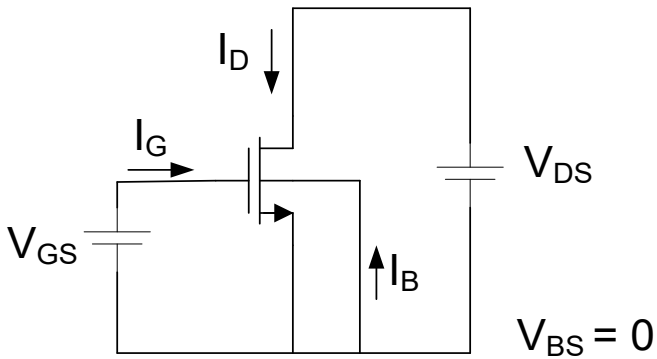
$$I_D = \frac{\mu C_{OX} W}{2L}\left(V_{GS} - V_{TH}\right)^2$$

$$I_G = I_B = 0$$

Model in Saturation Region

Model Summary

n-channel MOSFET



Notation change: $V_T = V_{TH}$, don't confuse V_T with $V_t = kT/q$

$$I_D = \begin{cases} 0 & V_{GS} \le V_{TH} \quad \text{Cutoff} \\ \mu C_{OX} \frac{W}{L}\left(V_{GS} - V_{TH} - \frac{V_{DS}}{2} \right) V_{DS} & V_{GS} \ge V_{TH} \quad V_{DS} < V_{GS} - V_{TH} \quad \text{Triode} \\ \mu C_{OX} \frac{W}{2L}\left(V_{GS} - V_{TH} \right)^2 & V_{GS} \ge V_{TH} \quad V_{DS} \ge V_{GS} - V_{TH} \quad \text{Saturation} \end{cases}$$

$$I_G = I_B = 0$$

Model Parameters: {μ, V_{TH}, C_{OX}} Design Parameters : {W, L}

This is a piecewise model (not piecewise linear though)

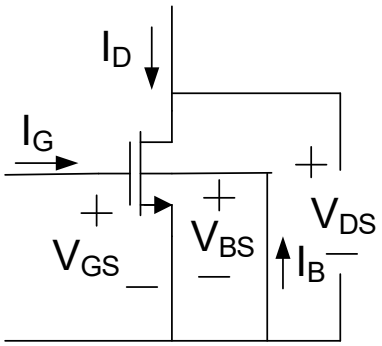
Piecewise model is continuous at transition between regions

(Deep triode special case of triode where V_{DS} is small $R_{CH} = \frac{L}{W} \frac{1}{\left(V_{GS} - V_{TH} \right) \mu C_{OX}}$)

Note: This is the third model we have introduced for the MOSFET

Model Summary

n-channel MOSFET



$V_{BS} = 0$

$$I_D = \begin{cases} 0 & V_{GS} \le V_{TH} \\ \mu C_{OX} \dfrac{W}{L}\left(V_{GS} - V_{TH} - \dfrac{V_{DS}}{2} \right) V_{DS} & V_{GS} \ge V_{TH} \quad V_{DS} < V_{GS} - V_{TH} \\ \mu C_{OX} \dfrac{W}{2L}\left(V_{GS} - V_{TH} \right)^2 & V_{GS} \ge V_{TH} \quad V_{DS} \ge V_{GS} - V_{TH} \end{cases}$$

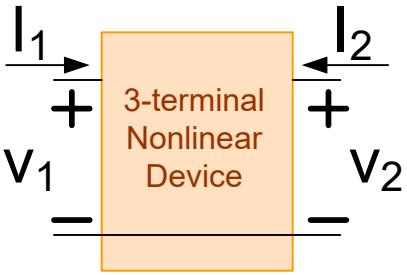
$$I_G = I_B = 0$$

Observations about this model (developed for V_{BS}=0):

$$I_D = f_1(V_{GS}, V_{DS})$$
$$I_G = f_2(V_{GS}, V_{DS})$$
$$I_B = f_3(V_{GS}, V_{DS})$$

This is a nonlinear model characterized by the functions f_1, f_2, and f_3 where we have assumed that the port voltages V_{GS} and V_{DS} are the independent variables and the drain currents are the dependent variables

General Nonlinear Models

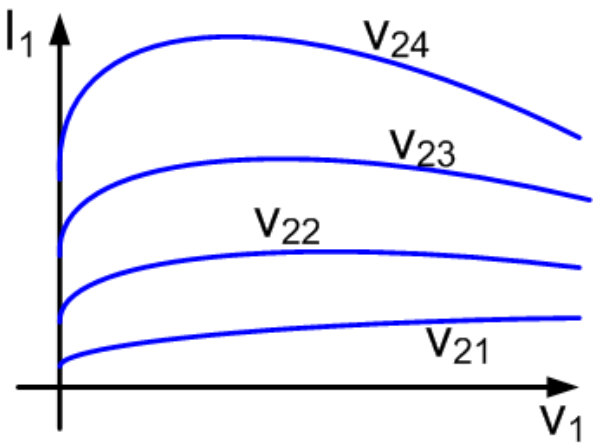


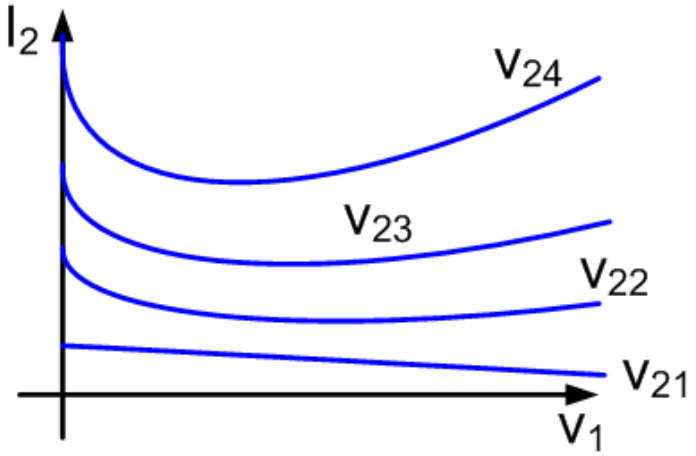
$$I_1 = f_1(V_1, V_2)$$

$$I_2 = f_2(V_1, V_2)$$

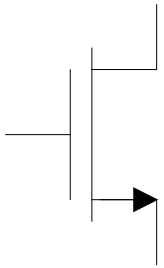
I_1 and I_2 are 3-dimensional relationships which are often difficult to visualize

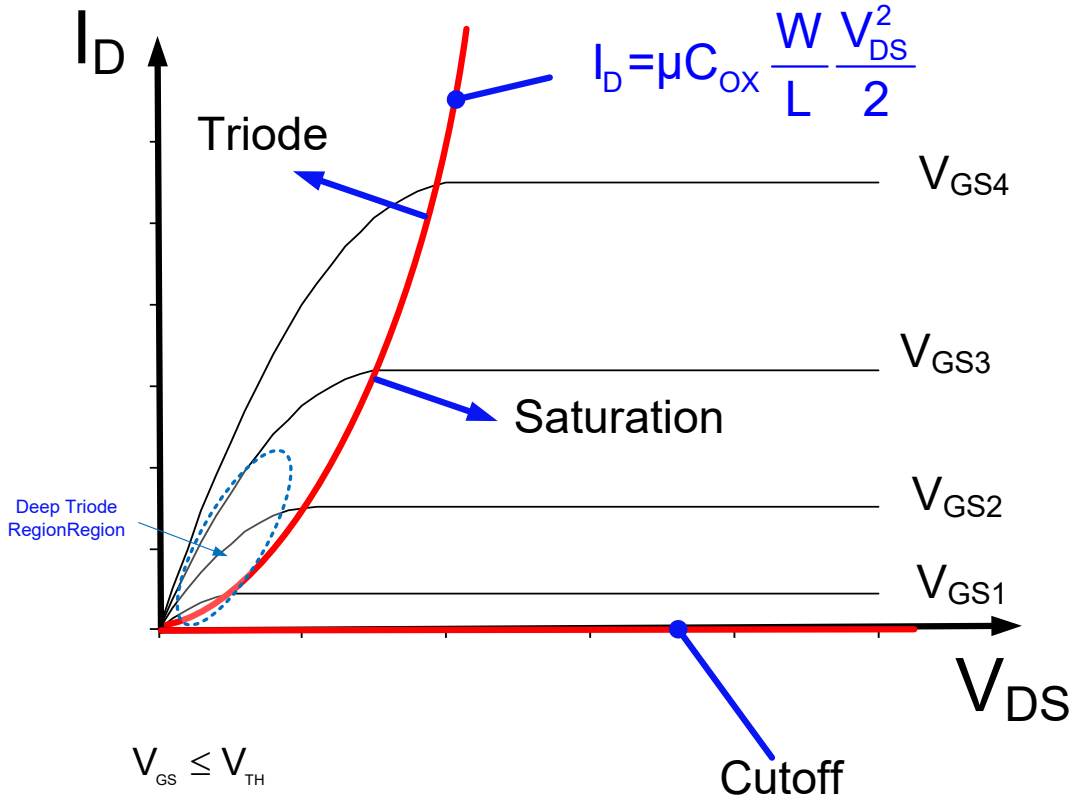
Two-dimensional representation of 3-dimensional relationships





Graphical Representation of MOS Model



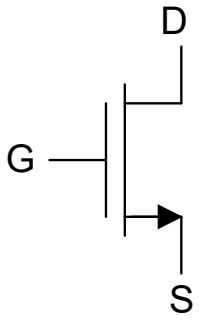


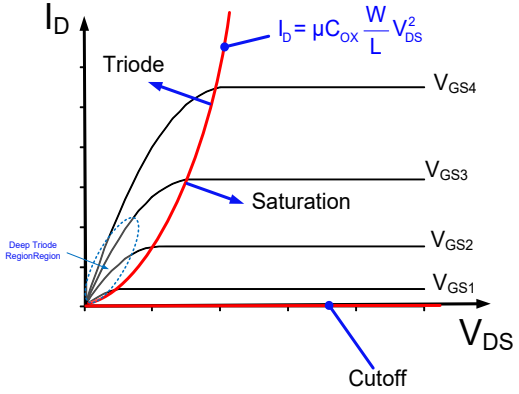
$$I_D=\begin{cases}0 & V_{GS}\le V_{TH}\\ \mu C_{OX}\frac{W}{L}\left(V_{GS}-V_{TH}-\frac{V_{DS}}{2}\right)V_{DS} & V_{GS}\ge V_{TH} \quad V_{DS}< V_{GS}-V_{TH}\\ \mu C_{OX}\frac{W}{2L}\left(V_{GS}-V_{TH}\right)^2 & V_{GS}\ge V_{TH} \quad V_{DS}\ge V_{GS}-V_{TH}\end{cases}$$

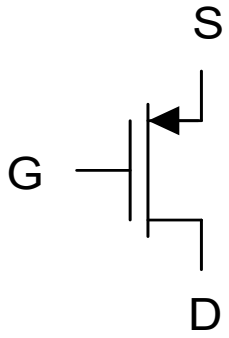
$I_G=I_B=0$

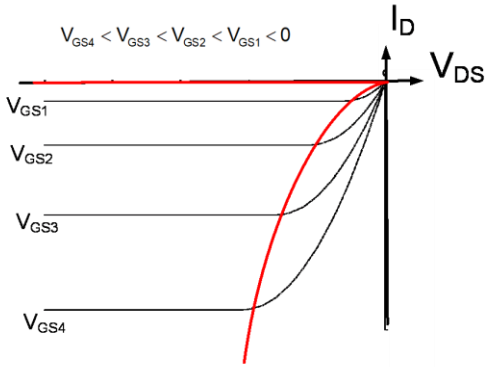
Parabola separated triode and saturation regions and corresponds to $V_{DS}=V_{GS}-V_{TH}$

PMOS and NMOS Models









- Functional form identical, sign changes and parameter values different
- Will give details about p-channel model later

Stay Safe and Stay Healthy !

End of Lecture 16